MPD Tech Note

MICROPOWER DIRECT

Driving Insulated Gate Bipolar Transistors (IGBT's)

MicroPower Direct

MPD, a leading worldwide provider of power conversion products, was founded by a group of industry veterans in 1999. Located in Stoughton, MA, we are committed to delivering innovative, high quality power converters at the lowest possible prices.

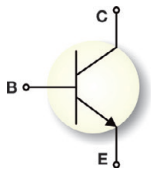
We currently offer over 5,000 low cost standard "off-the-shelf" high performance power converters. Our product lines include DC/DC converters, AC/DC power supplies, high brightness LED drivers, IGBT drivers & controllers, and switching POL regulators.

Component selection and layout are carefully considered at the design stage to optimize product reliability. All manufacturing is in ISO9000 registered factories under strict quality control system guidelines. All products are supported worldwide, and carry a standard three year warranty.

MPD power products have been designed into a wide variety of products and systems by a very diverse customer base. End products range from computer peripherals to test instrumentation to telecommunications equipment to process/industrial controls to medical devices and more.

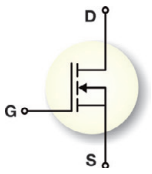
An ideal semiconductor power switch would be capable of very high switching speeds, have very low on-state conduction losses and have a drive/control circuit that is as simple as possible. There has been a great deal of effort over the years to develop or refine materials, process capabilities, and circuits that have steadily improved the performance of semiconductor switches. With this note, we will discuss three of the major semiconductors developed.

Until the early 1970's, the only real choice for power switching applications was the bipolar junction transistor (BJT). First invented in 1948, the BJT is a three layer (PNP or NPN) sandwich. At right is the symbol for an NPN BJT. While the BJT is capable of switching high currents at high speeds, it has significant disadvantages:



- **Current Control** - Base current is required to keep the the transistor in the "ON" state. Typically 10% to 20% of collector current) This can substantially increase power losses during operation.
- **Slow Turn Off** - For power switching applications, the BJT is slower than the MOSFET or IGBT. In applications where the collector voltage has to go to zero (or close to it), time is required to flush out minority carriers stored in the base during saturation.
- **Negative Temperature Coefficient** - This means that as the temperature of the BJT die rises it will conduct more current. Normal production flaws in the manufacture of the BJT die cause higher temperature levels at some areas of the die. The higher temp rise causes a higher current flow which in turn causes an increase in temperature. Left unchecked, this will lead to thermal runaway and eventually a failure mode known as "secondary breakdown". This may cause a catastrophic failure of the component.

In the 1970's, the development of the Metal Oxide Semiconductor Field Effect Transistor or MOSFET, addressed many of these issues (the circuit symbol at right is for an N-Channel MOSFET). The MOSFET is a unipolar transistor that operates as a voltage-controlled current device. It has four terminals; the source (S), gate (G), drain (D), and body (B). In practice, the body is typically connected to the source terminal (this is done internally), making the MOSFET a three-terminal device. The Gate is insulated from the semiconductor surface by a thin layer of oxide.



The MOSFET was quickly adopted for high speed switching applications. As compared to BJT's, the MOSFET has many advantages in these applications:

- **Voltage Control** - A voltage applied to gate terminal creates a conduction channel between the base and source through which current can flow. Since the current required is very low, drive circuits for the MOSFET are simpler and less expensive.
- **Higher Speed** - There is no current tail, so switching speeds are orders of magnitude higher than BJT's.
- **Positive Temperature Coefficient** - The forward-voltage drop of the MOSFET increases with an increase in temperature. This essentially eliminates the risk of thermal runaway.
- **Input Impedance** - The MOSFETs input impedance is very high, so "Loading Effect" is not an issue.

The MOSFET is also physically smaller than the BJT and is less affected by circuit noise. But, it does have some disadvantages. At high voltage levels, the source-drain resistance (R_{DSON}) increases, increasing conduction losses and lowering efficiency. As such, they are not a good choice for high voltage, high current (high power) applications. They are also susceptible to damage from electrostatic discharge.

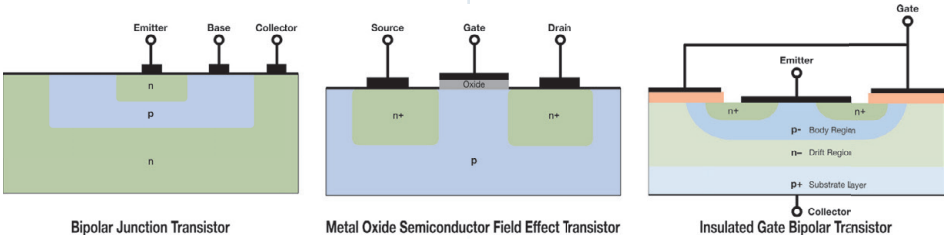
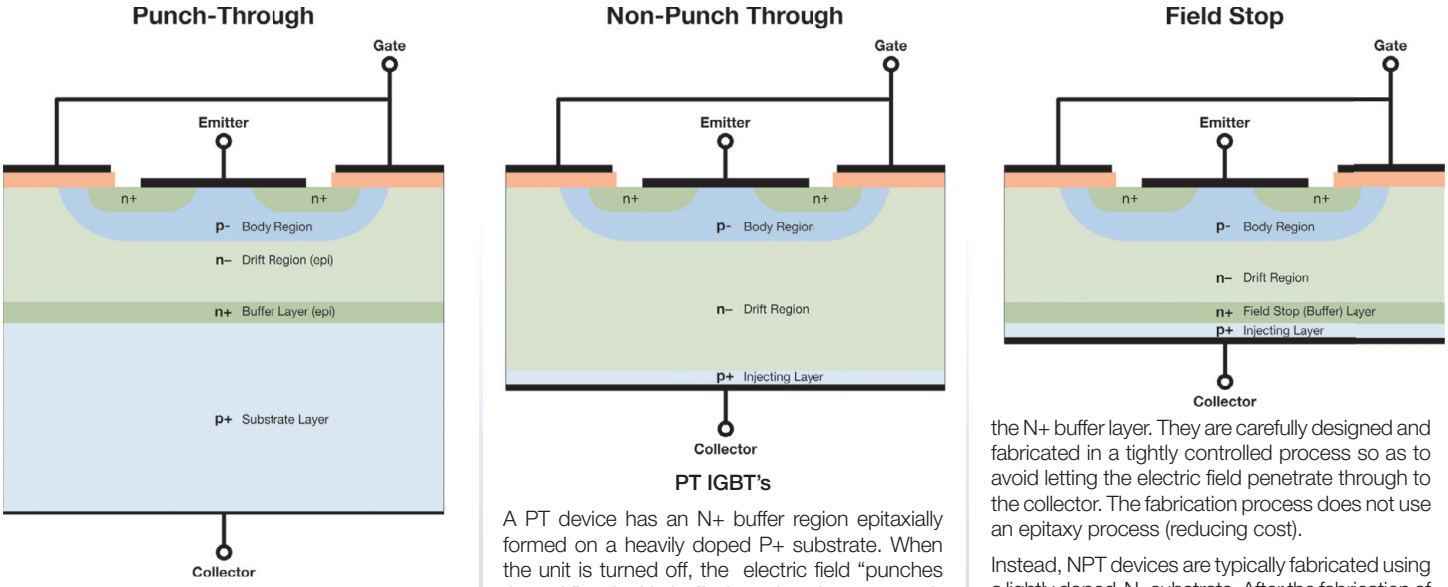
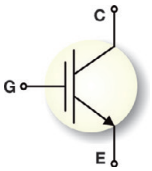


Figure 1 Cross Section Diagrams of Power Semiconductors

Figure 2 Cross Section Of Major IGBT Technologies



In the early 1980's, the Insulated Gate Bipolar Transistor (IGBT) was introduced. The IGBT combines features of the BJT and MOSFET. It has the simpler, voltage controlled gate drive of the MOSFET and the high current capability of the BJT. This combination has made the IGBT the preferred device for high power applications.



They share advantages & disadvantages of both devices:

- **Voltage Control** - Like the MOSFET, a voltage applied to gate terminal creates a conduction channel between the collector and emitter through which current can flow.
- **Power Rating** - The power handling capability is higher than the MOSFET or BJT. This is due to the low on-state collector-emitter resistance, and a high forward conduction current density.
- **Switching Speed** - The switching speed of the IGBT is limited by collector current tailing. Like the BJT this is caused by the need to "sweep out" minority carriers. IGBTs are slower than MOSFET's but faster than BJT's.

A quick comparison of the three devices is given in table 1.

Parameter	BJT	MOSFET	IGBT
Input Impedance	Low	High	High
Output Impedance	Low	Medium	Low
Input Drive	Current	Voltage	Voltage
Drive Power	High	Low	Low
Drive Circuit	Complex	Simple	Simple
Voltage Rating	High	High	Very High
Current Rating	High	Low	High
Switching Speed	Slow	Fast	Moderate
Safe Operating Area	Narrow	Wide	Wide

Table 1 Power Semiconductor Parameter Comparison

IGBT's are generally fabricated using one of three general techniques. As shown in figure 2, these manufacturing methods are punch-through (PT), non-punch-through (NPT) and Field Stop (FS).

PT IGBT's

A PT device has an N+ buffer region epitaxially formed on a heavily doped P+ substrate. When the unit is turned off, the electric field "punches through" to the N+ buffer layer, but does not reach the P+ substrate layer. This action completely depletes the N- drift region of carriers.

This results in a very thin N- drift region that minimizes $V_{CE(ON)}$ (turn-on voltage). The addition of the buffer layer also improves switching speed by reducing the number of excess holes that are injected into the P+ substrate. When the device is switched off, these carriers are quickly removed.

On the plus side, PT devices have a short tail current, low conduction losses and low switching losses. They are currently available up to 1200V, but are more commonly used 600V.

On the minus side, the fabrication process is more expensive and they are larger (wafer thickness). The heavily doped P substrate increases switching losses as frequency increases, limiting their use at higher switching speeds. They are also more temperature sensitive which makes paralleling difficult (sorting is required) and can significantly increase switching losses.

For PT devices, the forward breakdown voltage is higher than the reverse breakdown voltage (asymmetrical). They are primarily used in DC circuits where they do not see voltages in both directions.

Wafer Thickness

Wafer thickness is a physical parameter that has a considerable (if indirect) effect on a "Figure Of Merit" (FOM) that is often used as a performance index for evaluating IGBTs. The FOM is defined as:

$$\mathbf{FOM} = \frac{J_C}{V_{CE(SAT)} \times E_{OFF}}$$

Where JC = chip current density (A/cm^2)
$V_{CE(SAT)}$ = C - E saturation voltage
E_{OFF} = the turn off energy loss (mJ/pulse/A)

Reducing the wafer thickness lowers the saturation voltage (and conduction losses). A thinner wafer results in a shorter conduction path, reduces $V_{CE(SAT)}$ and improves the FOM. Wafer processing has been steadily improved from the introduction of 1ST generation planar products to fine patterning to "trench" products (introduced by the 4TH generation).

NPT IGBT's

The NPT was developed as an effort to improve on the PT architecture. As can be seen, it eliminates the N+ buffer layer. They are carefully designed and fabricated in a tightly controlled process so as to avoid letting the electric field penetrate through to the collector. The fabrication process does not use an epitaxy process (reducing cost).

Instead, NPT devices are typically fabricated using a lightly doped N- substrate. After the fabrication of

Latch Up

An IGBT is made of four alternate P-N-P-N layers. these layers form a parasitic thyristor which could latch on under certain conditions. The base of the "NPN" transistor is the body region. The P substrate and N drift and P body regions form the PNP transistor. If the "NPN" turns on and the gains of the "NPN" & "PNP" are >1, latch up will occur.

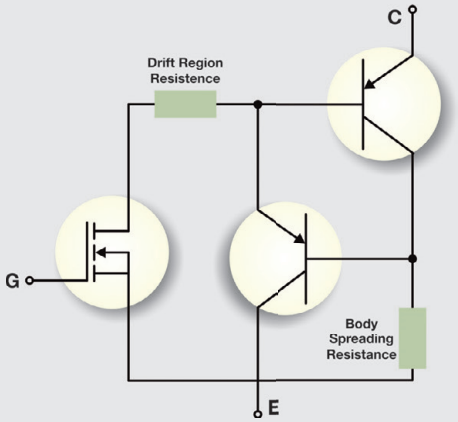


Figure 3 IGBT Equivalent Circuit

The body region is connected to the emitter to prevent it turning on. But, the body region does have some resistance (called spreading resistance). During the device On state, this resistance produces a voltage drop that, if large enough, could forward bias the N+ P junction. If transistor gains >1, static latch up occurs. During a high dv/dt turn on, excessive collector current could also increase the gains above 1 and latch on the parasitic thyristor. This is dynamic latch up (which can affect the device SOA). Once latch up occurs, the device will be destroyed by excessive power.

To avoid this, the doping levels & geometries of the body region have been made to reduce the gain of the lateral NPN (the center NPN in the equivalent circuit above) and lower the spreading resistance).Decreasing the gain of the vertical NPN would affect the V_{ON} voltage and conduction of the device negatively.

For all practical purposes, Latch Up has been eliminated as a problem in IGBT's produced now.

top structures, the back of the float-zone wafer is thinned (by mechanically grinding it) and polished. The p-layer on the collector side is then added by means of an implantation step.

NPT devices are typically lower cost than PT units, are more stable over temperature, easier to parallel and are short circuit rated. They are also more robust than PT devices. But, they do have higher switching and conduction losses.

For NPT devices, the forward breakdown voltage is equal to the reverse breakdown voltage (symmetrical). They are often used in AC circuits where they do see voltages in both directions.

Field Stop IGBT's

The Field Stop IGBT combines some of the qualities of the PT and NPT devices. They are fabricated similar to the NPT process (no epi), but a buffer (Field Stop) layer has been added back in. The drift region is now thinner, resulting in a lower V_{CESAT}.

Importantly, most field stop IGBTs are fabricated using "Trench" technology (many are actually called Trench Stop or Trench Gate). The gate structure on these devices is put into a vertical "trench") that extends into the drift region. The gate structure effectively shortens the conduction path (V_{CE} is proportional to the length of the conduction path). The conduction channel must be long enough to hold the break down voltage and hold the short circuit current without failing.

Parameter	PT	NPT	FS NPT
Conduction Losses	Low	Medium	Low
Switching Losses	Low	Medium	Low
Tail Current	Short	Long	Short
V_{CESAT}			
Voltage Rating	Medium	High	High
Reliability	Medium	High	High
Paralleling	Hard	Easy	Easy
SCSOA [1]	Medium	High	High

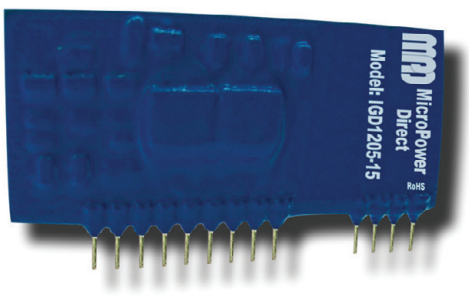
Table 2 IGBT Parameter Comparison

Note 1: Short Circuit Safe Operating Area

Parallel Operation & Free Wheel Diode

In many high power applications, IGBTs are placed in parallel to achieve very high-current operation. If these IGBTs have threshold or on-state voltage levels that are seriously mismatched, a very large current will flow to the IGBT with a relatively lower conduction value. To insure safe operation in a parallel connection, each IGBT should have as small a deviation as possible.

The structure of an IGBT does not include a body diode like that of a MOSFET. IGBT's used in circuits where reverse conduction occurs (such as bridge circuits) will need a blocking diode. Switching off



IGD1205W - Hybrid Integrated N-Channel IGBT Driver

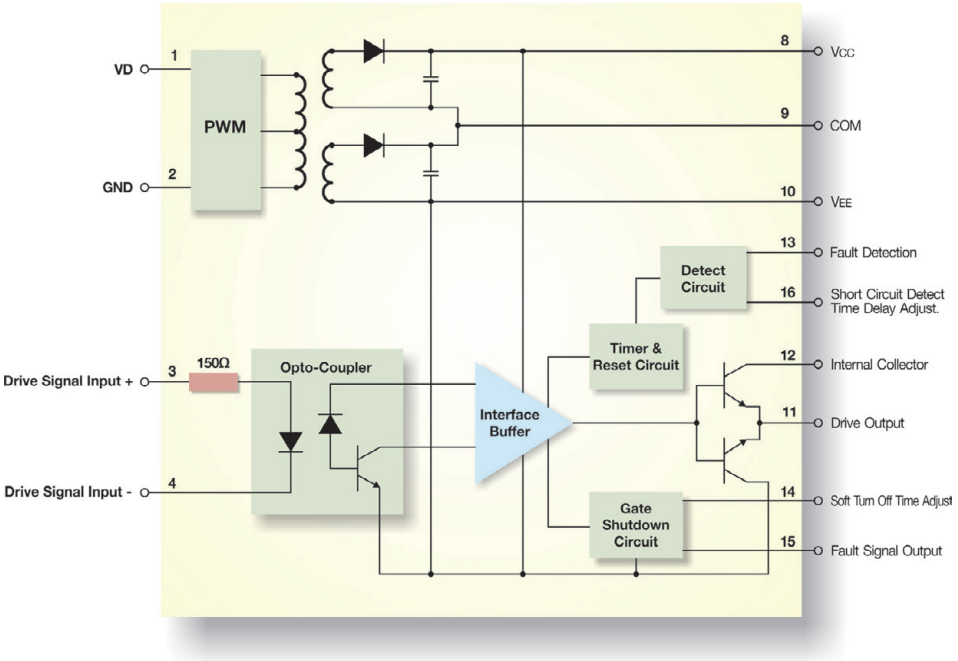


Fig 4 - IGD1205RW Block Diagram

an inductive load can generate high voltage peaks that would damage the device if a suitable bypass through the diode is not provided.

Driving the IGBT

IGBTs can be found in solar inverters, uninterruptible power systems, motor controls, high frequency welders and induction heating circuits to name just a few. They are often used in bridge circuits, both symmetrical and asymmetrical. Regardless of the specific application, the gate drive circuit is critical to achieving maximum system operation, efficiency and reliability. One way to simplify the design of the drive circuit is to use a hybrid controller like the **IGD1205W**.

The **IGD1205W** is a hybrid integrated circuit designed to provide the isolated gate drive required for high power IGBT modules. It features an internal high speed optocoupler, high transient immunity, short circuit protection and a fault signal output. It is packaged in a compact single-in-line (SIP) package (see below) that minimizes the required printed circuit board space. The block diagram (Figure 4) illustrates its' main components and features.

The **IGD1205W** converts logic level control signals into a fully isolated gate drive of +15V/-8V. Gate drive current is 5A peak. Gate drive power isolation is provided by an internal DC/DC converter. Control signal isolation is provided by an internal high speed optocoupler. Desaturation detection is used for short circuit protection.

An example application circuit for the **IGD1205W** is figure 6 (on page 4). The complete gate driver circuit can be constructed with as few as eleven external components. The external isolated power supply typically required for the gate drive circuit is not necessary, due to the built-in DC/DC converter included with the **IGD1205W**.

Control Power Supply

The **IGD1205W** requires a single 12 or 15 VDC control supply to power its internal circuits. The control power supply is connected to the primary side of the hybrid gate driver's built in DC/DC converter at pins 1 & 2. In our example circuit, we use an **MD2xxS-15E**, a low cost 2W DC/DC converter in a compact SIP package. The control power supply must be decoupled with a capacitor (C_3) mounted as close as possible to the driver's pins. The decoupling capacitor is necessary to provide a stable, well filtered voltage for the driver's built in DC/DC converter. When selecting the input decoupling capacitor, it is important to ensure that it has a sufficiently high ripple current rating.

In our example circuit (figure 6) we use a low impedance, 100 μF electrolytic for the input decoupling capacitor. This should be sufficient for most applications. If the driver is lightly loaded, It may be possible to use a smaller capacitor.

The current draw on the 15V converter will vary from about 50 mA to almost 100 mA depending on the size of the IGBT being driven and the switching frequency. The basic procedure is as follows:

1. **Determine the average gate drive current.** The average current required to drive the IGBT is a function of operating frequency, on and off bias voltages and total gate charge. The average current that must be supplied by the gate driver is given by:

$$I_{DRIVE} = Q_G \times f$$

Where: Q_G = total gate charge
f = frequency of operation

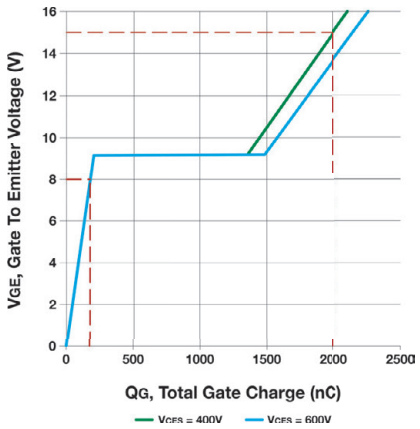
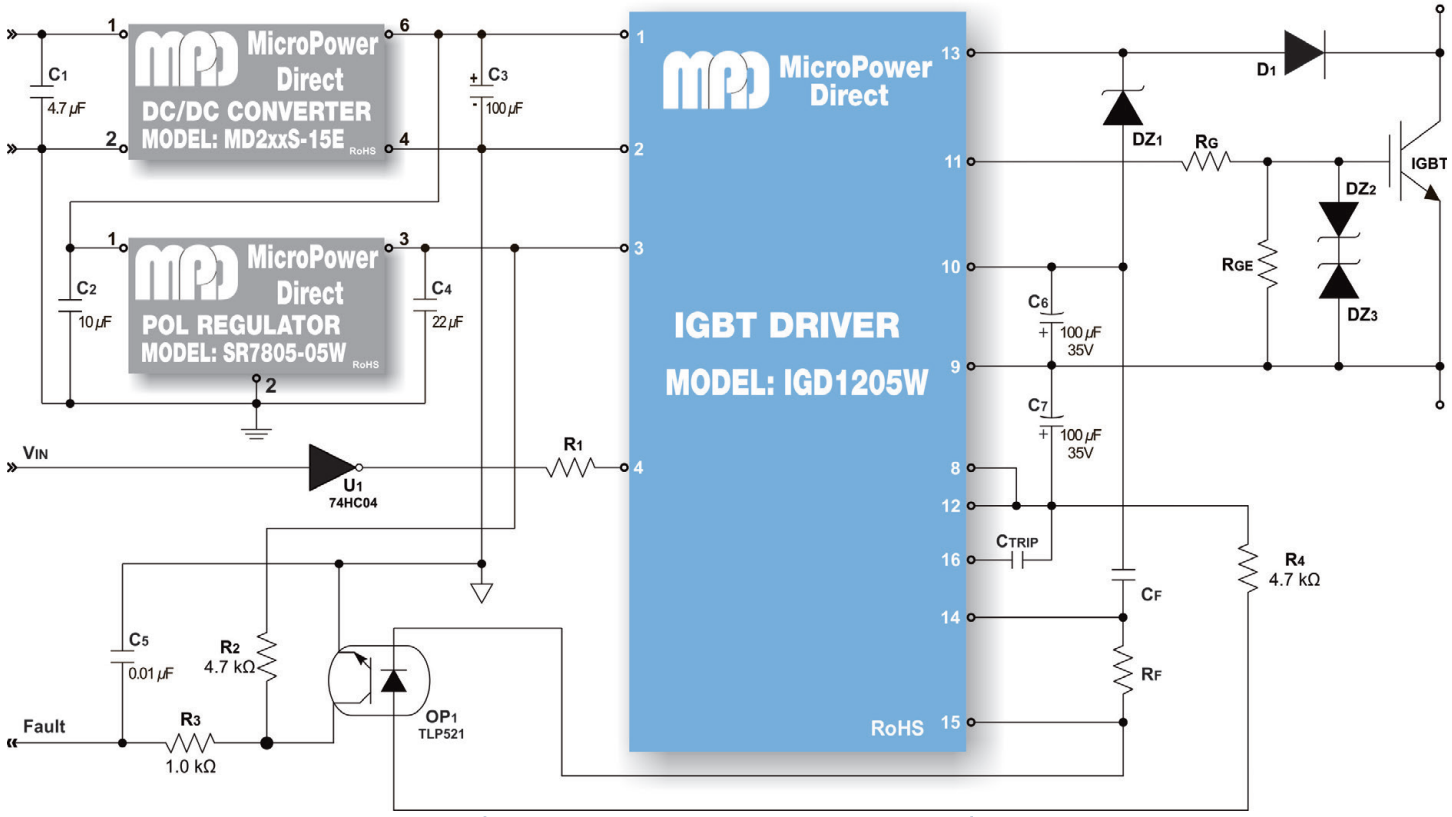


Fig 5 - Typical Total Gate Charge Curves

Figure 6 - IGD1205W Typical Application Connection



The IGBT module datasheet curves will give the total gate charge (fig 5 on page 3). For our example, the total gate charge for the gate voltage transition from 0V to +15V is 2,000 nC. The gate charge for the transition from 0V to -8V is an additional 200 nC. For operation of the device at 20 kHz the required supply current is:

I_{DRIVE} = (2,000 nC + 200 nC) x 20 kHz = 44mA

2. **Calculate the total gate drive power**
The power that must be supplied by the **IGD1205W**'s internal DC/DC converter is by given by:

$$P_G = I_{DRIVE} \times (V_{CC} + |V_{EE}|)$$

Where V_{CC} and V_{EE} are the DC/DC output voltages as specified on the driver datasheet. For our application example, V_{CC} = 15 VDC and V_{EE} = -8 VDC. Using these values, the gate drive power is equal to:

$$P_G = 44\ mA\ (15V + |-8V|) = 1W$$

3. **Calculate the input power required.**
The total power required from the input power source (the **MD2xxS-15E** in our example) is equal to the total gate drive power (P_G) divided by the **IGD1205W** efficiency, which is about 80%. The required total input power is calculated using this efficiency as follows:

$$P_T = \frac{P_G}{Eta} = \frac{1.0W}{0.8} = 1.25W$$

4. **Calculate the input current required.**
The required input current is simply the total input power required (**P_T**) divided by the supply voltage.

$$I_D = \frac{P_T}{V_D} = \frac{1.25W}{15V} = 83\ mA$$

No	Component	Typical Value	Description	See Note
1	D_1	0.5A	V_{CE} detection diode	1
2	D_{Z1}	30V, 0.5W	Fault detection Input surge voltage protection	2
3	D_{Z2}, D_{Z3}	18V, 1.0W	Gate surge voltage protection	
4	C_3	100 µF/35V	Control power supply decoupling	3
5	C_6, C_7	100 -1,000 µF/35V	DC/DC Output filter	4
6	C_5	0.01 µF	Fault feedback signal noise filter	
7	C_F	0 - 10 nF	Soft shut-down adjust, multilayer ceramic or film	
8	C_{TRIP}	0 - 3,300 pF	Trip time adjust, multilayer ceramic or film	
9	R_F	100Ω - 1.5 kΩ	Soft shut down adjustment	
10	R_4	4.7 kΩ, 0.25W	Fault sink current limiting resister	
11	R_2	4.7 kΩ, 0.25W	Fault feedback signal pullup	
12	R_3	1.0 kΩ, 0.25W	Fault feedback signal noise filter	
13	R_1	See Note 5	Input signal current limiter	5
14	OP_1	TLP521	Optocoupler for fault feedback signal isolation	
15	U_1	CMOS Buffer	74HC04 or similar	6

Notes:
1. The V_{CE} detection diode should have a blocking voltage equal to or greater than the V_{CES} of the IGBT being driven. The diode recovery time should be less than 200 nS to prevent high voltage being applied to pin 13.
2. The diode D_{Z1} protects pin 13 from voltage surges during the recovery of D_1.
3. The decoupling capacitor for the control power supply should be mounted as close to the input pins of the gate driver as possible.
4. The DC/DC output capacitors must be selected to have the appropriate ESR and ripple current capability for the IGBT being driven.
5. See section "Input Circuit" on page
6. The CMOS buffer must actively pull high to maintain noise immunity.

The **MD2xxS-15E** operates from input bus voltages of 5, 12, or 24 VDC. The "-15" models have a 15 VDC output rated at 133 mA.

Input Circuit

As can be seen in the block diagram (figure 4) the drive signal input circuit, between pins 3 and 4, consists of a 150Ω resistor in series with the built in high speed optocoupler's LED. When a 5V control signal is applied to pin 4, approximately 18 mA of drive current is supplied for the optocoupler.

In most applications pin 3 will be tied directly to a 5V power supply. In our example (figure 6) we use the **SR7805-05W** a low cost point of load (POL) regulator to convert the 15V output of the **MD2xxS-15E** to a well regulated +5 VDC.

Capacitor C_2 is a low ESR ceramic 10 μF/50V capacitor used to help stability (of the POL) and to minimize noise at the regulator input. A tantalum or low ESR electrolytic capacitor may also be used. Capacitor C_4 is a 22 μF ceramic used to reduce ripple at the regulator output. Both capacitors should be mounted as close to the regulator pins as possible.

An ON signal (gate output high) is generated by pulling pin 4 to ground. A CMOS buffer capable of sinking up to 18 mA is required. The 74HC04 hex inverter (or a similar component) is used here. In the off state, the buffer (U_1) should actively pull pin 4 high to maintain good noise immunity. An open collector drive is not recommended because allowing pin 4 to float will degrade common mode noise immunity.

If a different control voltage (other than 5V) is required, an external current limiting resistor (R_1) must be added. A good example of this would be if we eliminated the switching POL regulator (the **SR7805-05W**) and tied pin 3 directly to the +15V output of the **MD2xxS-15E**. The value of the external resistor would then be calculated by the following formula:

$$R_1 = \frac{V_{DR} - V_{OFD} - V_{OSD}}{18\ mA} - 150\Omega$$

Where: V_{DR} = Required drive voltage
V_{OFD} = Forward voltage drop across Opto-coupler diode
V_{OSD} = On state voltage drop across the driver

If we assume that V_{OFD} is 1.5V and V_{OSD} is 0.6V; for a driver voltage of 15V the current limiting resistor would be equal to:

$$R_1 = \frac{15V - 1.5V - 0.6V}{18\ mA} - 150\Omega = 510\Omega$$

To maintain good noise immunity, this resistor (R_1) should always be connected in series with pin 4. The common mode noise immunity of the gate driver will degrade if it is connected in series with pin 3.

Isolation Power Supplies (V_{CC} and V_{EE})

The **IGD1205W** has a built in DC/DC converter that provides isolated gate driver voltage levels consisting of +15V (V_{CC}) at pin 8 and -8V (V_{EE}) at pin 10. The V_{CC} level (+15V) is high enough to fully saturate the IGBT, minimizing on-state losses. At the same time it's low enough to limit short circuit current.

When its gate voltage is at zero, an IGBT is turned off. However, a reverse bias should be applied to insure the gate remains off. Otherwise, the presence of dv/dt noise (or other interference) could result in the IGBT turning on. The -8V (V_{EE}) should be sufficient to prevent this. The use of reverse bias to turn off the IGBT could also reduce turn-off losses.

These outputs share a common ground at pin 9. Transformer coupling provides 4,000 V_{RMS} isolation between the 15V control supply input (V_D) and the gate drive power.

This allows the **IGD1205W** to provide a completely floating gate drive, suitable for high or low side switching. The low impedance electrolytic capacitors C_6 and C_7 decouple the gate drive power supplies. Two specifications are critical when choosing these capacitors. The first is impedance. The **IGD1205W** is designed to operate with gate resisters (R_G) as low as 2.0Ω. Standard 100 μF capacitors can have an internal resistance of 1.0Ω or higher. Obviously this would limit the peak gate driving current to an unacceptable level. Therefore, low impedance capacitors are necessary to deliver high peak gate current.

Additionally, because of internal heating, electrolytic capacitors have a maximum allowable ripple current specification. If this specification is exceeded, the life expectancy of the capacitor can be significantly reduced. To estimate the ripple current requirements for capacitors C_6 and C_7, it is necessary to measure or calculate the RMS gate drive current.

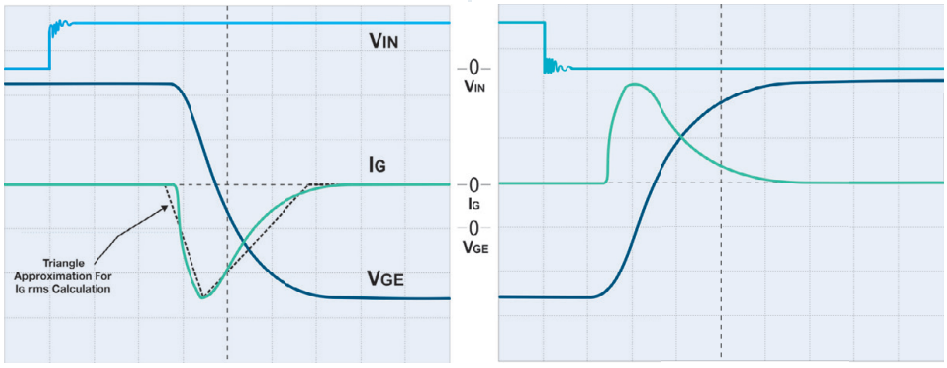
When measuring RMS gate current, the sampling rate of the test instrument must have a sampling rate that is high enough to accurately resolve the narrow gate current pulses. Most DMMs are not capable of measuring the measurement accurately.

The RMS gate current can also be estimated from the gate drive waveform. Figure 7 shows a typical gate current waveform. If it's assumed that the turn on/turn off pulses are approximately triangular, we can estimate RMS gate current using the following equations:

EQ 1. RMS current for repetitive triangular pulses

$$i_{RMS} = I_P \sqrt{\frac{T_P \times f}{3}}$$

Where: I_P = Peak current
T_P = Base width of pulse
f = Frequency



V_{IN}: 5V/div, I_G: 5A/div. T: 400 nS/div, R_G = 1.0Ω, C_L = 0.33 μF

Figure 7 - Typical Gate Current & Voltage Waveform

EQ 2. RMS current for Turn-On gate pulses

$$I_{G(ON)}\ (RMS) = I_{p(on)} \sqrt{\frac{T_{p(on)} \times f}{3}}$$

Where: $I_{P(on)}$ = Peak Turn-On current
$T_{P(on)}$ = Base width of On pulse
f = Frequency

EQ 3. RMS current for Turn-Off gate pulses

$$I_{G(OFF)}\ (RMS) = I_{p(off)} \sqrt{\frac{T_{p(off)} \times f}{3}}$$

Where: $I_{P(off)}$ = Peak Turn-Off current
$T_{P(off)}$ = Base width of Off pulse
f = Frequency

EQ 4. Total RMS gate current

$$I_{G(RMS)} = \sqrt{I_{G(on)(RMS)}^2 + I_{G(off)(RMS)}^2}$$

If we assume that the on & off pulses are symetrical, the RMS gate current is equal to:

$$I_{G(RMS)} = I_P \sqrt{\frac{2 \times T_P \times f}{3}}$$

Where I_P = Peak current
T_P = Base width of gate drive pulse
f = Frequency

Referring to figure 6 it can be seen that positive gate pulses are supplied by C_7 while negative gate pulses are supplied by C_6. For most applications the peak gate current is much larger than the average current supplied by the DC/DC converter. Given this, it is reasonable to assume that the RMS ripple current in the decoupling capacitors is roughly equal to the RMS gate current.

With this assumption, the ripple current in the decoupling capacitors (C_6, C_7) can be estimated using equations. For example, if a triangular approximation of the turn off pulses has the following measurements:

$I_{P(off)}$ = 5A
$T_{P(off)}$ = 1,500 nS
f = 20 kHz

Then the approximate ripple current in C_6 is equal to:

$$I_{G(OFF)}\ (RMS) = I_{p(off)} \sqrt{\frac{T_{p(off)} \times f}{3}}$$

Which in turn is equal to:

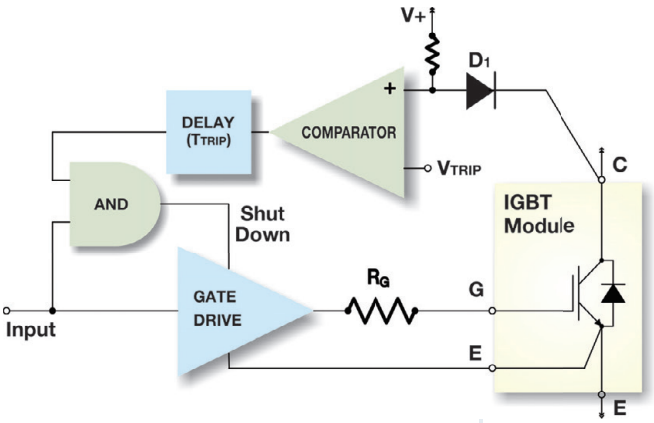
$$I_{G(OFF)}\ (RMS) = 5 \sqrt{\frac{1{,}500n \times 20k}{3}} = 0.5A$$

Generally it is a good idea to select a capacitor with a maximum ripple current rating higher than the calculated current. If the application is operating at lower frequency or lower peak current (larger R_G) it is possible to reduce the size of the decoupling capacitors C_6 and C_7. However, while capacitors with lower ripple current ratings may be smaller in size and lower in cost, the larger ones will have a longer life.

Gate Drive and Resistance (R_G)

The V_{EE} and V_{CC} supplies are connected to the driver's output stage to produce gate drive at pin 11. The gate drive current is adjusted by selecting the appropriate series gate resistance (R_G). The gate resistor must also be suitable for the IGBT module being used. A smaller gate

Figure 8 - Desaturation Detector Circuit



resistor will provide faster switching and lower losses while a larger gate resistor will reduce transient voltages and switching noise.

Typically, larger modules will require a smaller R_G and smaller modules will use a larger R_G. For most applications the optimum size of R_G will be somewhere between the data sheet value and ten times that value.

Keep in mind that the minimum R_G value allowable for the **IGD1205W** is 2.0Ω. An R_G of less than 2.0Ω could cause the peak output current to exceed the 5A maximum limit for the driver.

When driving large IGBT modules at high frequency, the power dissipated in the series gate resistor R_G can be substantial. Again, if we assume $I_G(on) = I_G(off)$, the approximate RMS gate current is:

$$I_{G(RMS)} = I_P \sqrt{\frac{2 \times T_P \times f}{3}}$$

Where I_P = Peak current
T_P = Base width of gate drive pulse
f = Frequency

The total power dissipation of the gate resistor Rg is:

$$I_{G(RMS)} = I_P \sqrt{\frac{2 \times T_P \times f}{3}}$$

For this example, at least a 3W resistor is required. The gate drive circuit layout must be designed so that the additional heat produced by the gate resistor does not overheat nearby components.

Protecting the gate against voltage surges are back to back zener diodes DZ_2 and DZ_3 as shown in figure 6. The diodes also help control short circuit currents by shunting miller current away from the gate. They must be capable of supporting high pulse currents, so diodes with a minimum 1W rating are recommended.

Short Circuit Protection

Most IGBT modules are designed to survive a low impedance short circuit for a minimum of 10 μs. The **IDG1205W** uses this capability to provide fast acting protection as part of the gate drive circuit. Implementing the protection as part of the gate drive circuit improves the speed of the circuit response by eliminating the propagation delays of the controller.

The **IDG1205W** provides short circuit protection by means of an on-state collector-emitter voltage sensing circuit. This type of protection is often called “Desaturation Detection”. A block diagram of a typical desaturation detector is illustrated in figure 8. In this circuit, a high voltage fast recovery diode (D_1) is connected to the collector of the IGBT to monitor the collector-emitter voltage.

When the IGBT is in the off state, V_{CE} is high and D_1 will be reverse biased. With D_1 off, the (+) input of the comparator is pulled up to the positive gate drive voltage (V_{DR}), which is normally +15V. When the IGBT turns on, the (+) input of the comparator will be pulled down by D_1 to the IGBT’s $V_{CE\,(sat)}$.

The (-) input of the comparator is supplied with a fixed voltage (V_{TRIP}). During a normal on-state condition the comparator’s (+) input will be lower than V_{TRIP} and the comparator output will be low. During a normal off-state condition the comparator’s (+) input will be higher than V_{TRIP} and the comparator output will be high. If the IGBT turns on into a short circuit, the high current will cause it’s collector-emitter voltage to rise above the level of V_{TRIP}, even though the gate of the IGBT is being driven on.

This condition (a high V_{CE} when the IGBT is supposed to be on) is often called desaturation. Desaturation can be detected by a logical AND of the **IDG1205W** input signal and the comparator output. When the output of the AND goes high a short circuit is indicated. The output of the AND can then be used to command the IGBT to shut down. A delay (T_{TRIP}) must be provided after the comparator output to allow for the normal turn-on time of the IGBT. This delay is set so that the IGBT’s V_{CE} has enough time to fall below V_{TRIP} during normal turn-on switching. If the delay is set too short, erroneous desaturation detection will occur. The maximum allowable delay is limited by the IGBT’s short circuit withstanding capability.

The recommended limit for a typical application is 10 μs. The **IGD1205W** incorporates short circuit protection using desaturation. Figure 9 illustrates the logical operation of the circuit shown. When desaturation is detected the gate driver performs a soft shut down of the IGBT and starts a 1.4 ms lock out period (T_{TIMER}). The soft turn off helps to limit the transient voltage that may be generated while interrupting the large short circuit current flowing in the IGBT. During the lock out the driver pulls pin15 low to indicate the fault status. Normal operation of the driver will resume after the lock out time has expired and the control input signal returns to the off state.

Trip Time Adjustment

The **IGD1205W** has a default short circuit detection time delay (T_{TRIP}) of about 1.6 μs. As long as the gate resistor (R_G) is near the minimum recommended for the IGBT module, this will prevent erroneous detection of short circuit conditions.

However, in some low frequency applications it may be desirable to use a larger gate resistor to slow the switching of the IGBT, reduce noise, and/or limit turn off transient voltages. When R_G is increased, the switching delay time of the IGBT will also increase. If this delay is too long,

Figure 9 - Desaturation Detector Operation

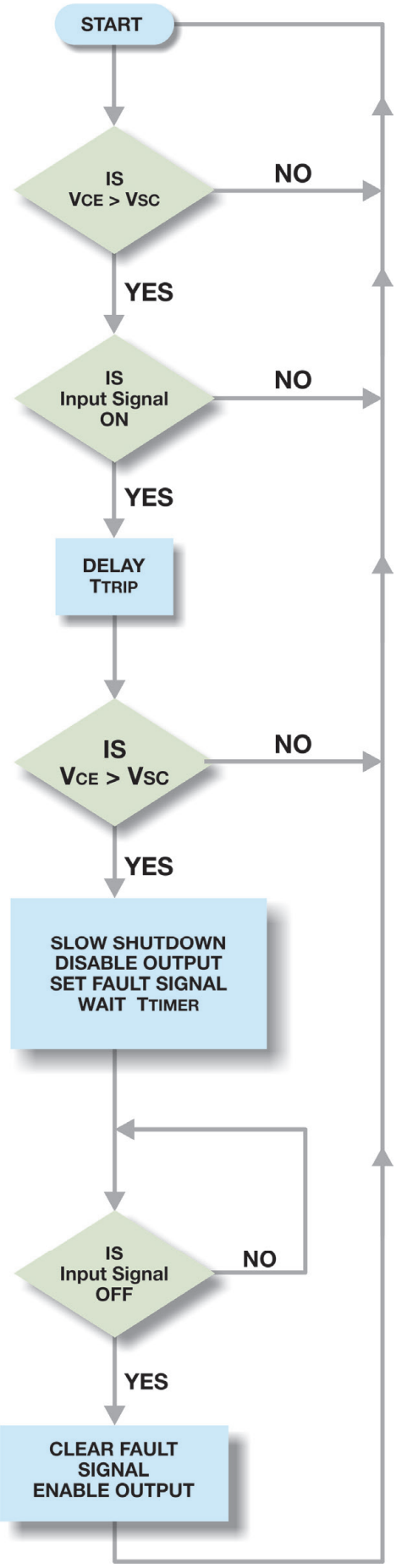


Figure 11 - Short Circuit Trip Delay Vs C_{TRIP}

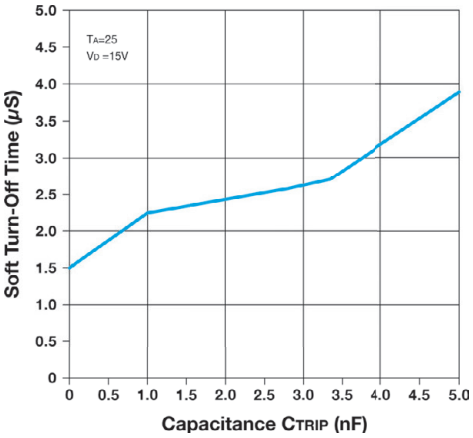


Figure 12 - Soft Turn-Off Speed Vs C_F

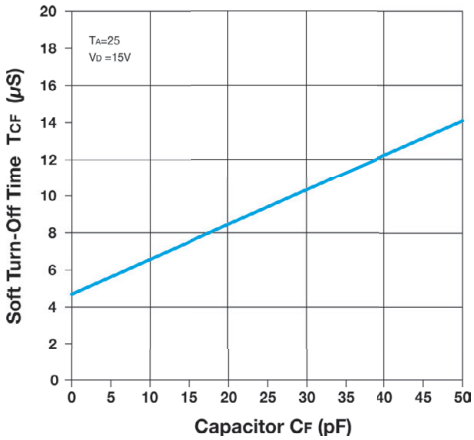
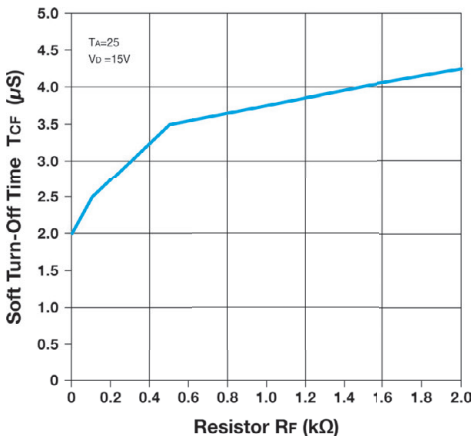


Figure 13 - Soft Turn-Off Speed Vs R_F



the detection circuit could indicate an erroneous short circuit.

To avoid this, the time delay (T_{TRIP}) can be extended by connecting a capacitor (C_{TRIP}) between pin 16 and V_{CC} (pin 8). The trip time as a function of C_{TRIP} is shown in figure 11. If T_{TRIP} is extended care must be exercised not to exceed the short circuit withstanding capability of the IGBT module. The short circuit detection time delay should not exceed 3.5 µs.

Adjustment of Soft Shut Down Speed

As noted, the **IGD1205W** provides a soft shut down when a short circuit is detected. This will help limit the transient voltage surge that occurs when large short circuit currents are interrupted. The default soft shutdown time is 4.5 µs. This setting will work for most applications

In applications using large modules or modules connected in parallel, it may be helpful to make the shut down even softer to minimize transient voltages. This can be done by connecting a capacitor (C_F) between pins 14 and 10. The speed of the shut down as a function of C_F is shown in figure 12.

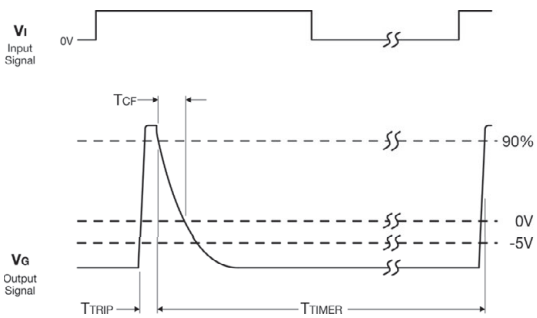
In applications using smaller IGBT modules, the softer shut down speed should be higher. A resistor (R_F) between pins 14 and 15 is required. The speed of the shut down as a function of R_F is shown in figure 13.

The soft shutdown time should be set between 2.5 µS and 10 µS. The capacitor C_F and resistor R_F should not be connected at the same time.

Short Circuit Protection Disable

In some applications it may be necessary or desirable to disable the short circuit protection function of the **IGD1205W**. This can be accomplished by connecting a 4.7 kΩ resistor from pin 13 to pin 9. This will force a low voltage on the detect input (pin 13) which in turn will prevent the driver from detecting desaturation. This is useful if the short circuit protection is not needed in an application. If the short circuit protection is disabled, the diode D_1 and the zener DZ_1 shown in figure 6 can also be omitted. Disabling the short circuit protection may also be desirable during initial circuit evaluation. With the short circuit protection disabled the drivers output will respond as expected to the input signal when the IGBT is not connected.

Figure 10 - T_{TRIP} Delay & Soft Shut Down



Fault Signal

If the **IGD1205W**'s short circuit protection is activated, it will immediately shut down the gate drive and pull pin 15 low to indicate a fault. Current flows from V_{CC} (pin 8) through the LED in the fault isolation optocoupler (OP_1) to pin 15. The transistor in the fault isolation optocoupler turns on and pulls the fault signal line low. During normal operation the collector of the optocoupler (OP_1) is pulled high to +5V at the output of the POL regulator, by the resistor R_2.

When a fault is detected the hybrid gate driver disables the output and produces a fault signal for a minimum of 1mS. Any signal on the fault line that is significantly shorter than 1mS is not a legitimate fault so it should be ignored. Therefore, for a robust noise immune design, it is recommended that an RC filter with a time constant of about 10 µs be added. In our circuit (figure 6) this filter is C_5 and R_3.

This opto isolated fault signal can now be used by the controller to detect a fault condition. If the short circuit protection function is not being used and has been properly disabled OP_1 and R_2 can be omitted and pin 15 left open.

Safe Operating Area

For high power semiconductors, such as an IGBT, the safe operating area (SOA) is defined as the voltage/current conditions over which the device is expected to operate without damage. The SOA is typically presented in graphical form, with performance curves illustrating the operating limits of the device.

For an IGBT, the SOA is the area bounded by a curve of collector current (I_C) vs collector to emitter voltage (V_{CE}). The curve gives the device current and voltage limits as they relate to the total power dissipation of the device. The device will operate without damage if the application does not exceed the SOA conditions. Somtimes the SOA of the IGBT is referred to as the "Forward Bias Safe Operating Area" (FBSOA). This is typically done to distinguish it from the RBSOA.

While turning off, IGBTs could also be damaged. The safe operating area for this period is called the Reverse Bias Safe Operating Area (RBSOA). It is important to consider the snubber (if present) operation during shutdown when considering RBSOA. Typically the RBSOA will be specified for a variety of turn-off conditions.

An IGBTs' Short Circuit Safe Operating Area gives the maximum duration of a short-circuit current pulse (under specified conditions). Exceeding this may cause the device to fail (typically by over-heating). The SCSOA is sometimes referred to as the SCWT (Short Circuit Withstand Time).

Driver Connection Tips & Cautions

Finally, a few comments on connections to the IGBT circuit. Care must be taken with circuit layout and the routing of wires not to induce unwanted noise and/or trigger unwanted switching of the IGBT. A few tips would include:

1. Keep printed circuit board traces as short as possible.
2. If cables are used to connect the driver to the IGBT, the cables should be kept as short as possible. Wiring to the gate and emitter should be twisted pair to minimize mutual induction.
3. Use twisted pair cables where possible
4. The signal cable should be kept away from power cables or a power terminal
5. In applications using multiple IGBTs, wiring for multiple devices should not be bundled together.
6. If used, the suppressor Diodes (DZ_2 & DZ_3) should be mounted as close to the IGBT as possible.
7. Board layout should include power traces & connections that are short and thick to reduce stray inductance.
8. Shielded cables should be used in noisy environments.

With this note, we have tried to present an overall look at the advantages and development of IGBTs;and some of the issues faced in using them. And more specifically, their use with hybrid drivers like the **IGD1205W**. If you have any questions or comments on this note or the **IGD1205W** driver, please contact technical sales at 781-344-8226.

MicroPower Direct: IGBT/SiC Products

IGBT DC/DC's

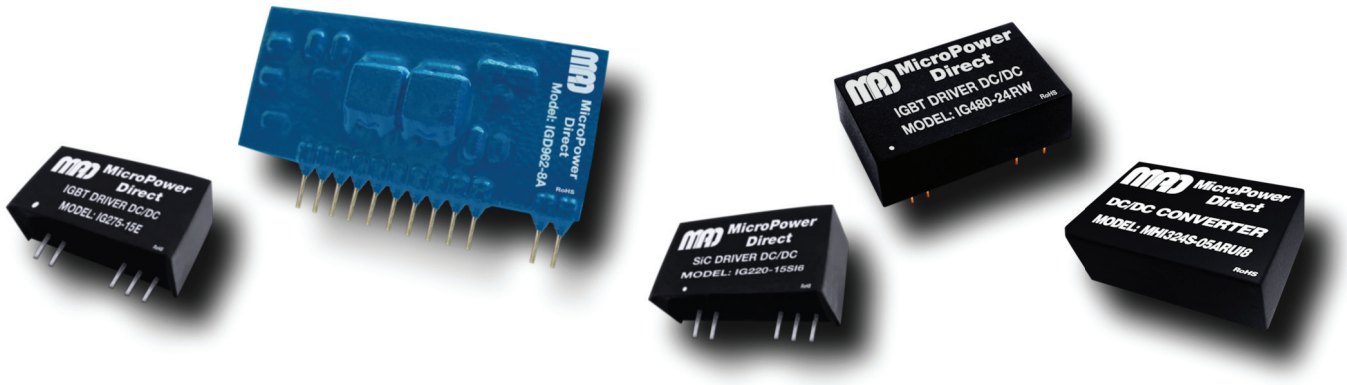
Model No	Power	Input Voltage		Isolation	+Output Voltage		-Output Voltage		Package Type
		Nominal	Range		VDC	mA	VDC	mA	
IG120-12	1.00W	12 VDC	±3.3%	3 kVAC	+15	+80	-8.7	-40	7-Pin SIP
IG120-12W	1.50W	12 VDC	±25%	3 kVAC	+15	+100	-8.0	-80	7-Pin SIP
IG120-15	1.50W	15 VDC	±10%	3 kVAC	+15	+80	-8.7	-40	7-Pin SIP
IG100-09	1.00W	15 VDC	±10%	3 kVAC	+9.0	+110	---	---	7-Pin SIP
IG100-09D	1.00W	15 VDC	±10%	3 kVAC	+9.0	+55	-9.0	-55	7-Pin SIP
IG136-15	1.70W	15 VDC	±10%	3 kVAC	+17	+80	-8.7	-40	7-Pin SIP
IG275-12E	2.76W	12 VDC	±5%	3 kVAC	+15	+120	-8.0	-120	7-Pin SIP
IG275-15E	2.76W	15 VDC	±5%	3 kVAC	+15	+120	-8.0	-120	7-Pin SIP
IG275-24E	2.76W	24 VDC	±5%	3 kVAC	+15	+120	-8.0	-120	7-Pin SIP
IG480-12RW	4.80W	12 VDC	2:1	3 kVAC	+15	+200	-9.0	-200	MiniDIP
IG480-24RW	4.80W	24 VDC	2:1	3 kVAC	+15	+200	-9.0	-200	MiniDIP

SiC DC/DC's

Model No	Power	Input Voltage		Isolation	+Output Voltage		-Output Voltage		Package Type
		Nominal	Range		VDC	mA	VDC	mA	
IG120-20	2.4W	15 VDC	±10%	3.5 VAC	+20	+100	-4.0	-100	7-Pin SIP
IG220-12	2.4W	12 VDC	±10%	3.5 VAC	+20	+100	-4.0	-100	7-Pin SIP
IG220-15	2.1W	15 VDC	±10%	3.5 VAC	+18	+100	-3.0	-100	7-Pin SIP
IG220-24	2.4W	24 VDC	±10%	3.5 VAC	+20	+100	-4.0	-100	7-Pin SIP

IGBT Drivers

Model No	Gate Voltage		CMR	Drive Channels	Isolation	Peak I_{OUT}	Package Type
IGD962-5A	+15 VDC	-5 VDC	30 kV/μS	One	3.75 kVAC	±5A	SIP
IGD962-8A	+15 VDC	-10 VDC	30 kV/μS	One	3.75 kVAC	±6A	SIP
IGD1205W-12	+16 VDC	-8.5 VDC	30 kV/μS	One	3.75 kVAC	±5A	SIP
IGD1205W-15	+16 VDC	-8.5 VDC	30 kV/μS	One	3.75 kVAC	±5A	SIP
IGD1208W-15	+16 VDC	-8.5 VDC	30 kV/μS	One	3.75 kVAC	±8A	SIP



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